

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

van der Goes *et al.*

Appl. No.: *To Be Assigned*  
(Continuation of Appl. No. 10/359,201;  
Filed: February 6, 2003)

Filed: *Herewith (July 24, 2003)*

For: **Subranging Analog to Digital  
Converter with Multi-Phase Clock  
Timing**

Art Unit: *To Be Assigned*

Examiner: *To Be Assigned*

Atty. Docket No: 1875.2820002/RES/GSB

**Preliminary Amendment**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Applicants submit the following Preliminary Amendment and Remarks. This Amendment is provided in the following format:

(A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;

(B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.121 and MPEP § 714; and

(C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

***Amendments***

***In the specification:***

Please substitute the following paragraph for pending paragraph [0001]:

--This application is a continuation of Application No. 10/359,201, filed on February 6, 2003, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der GOES *et al*, which is a continuation of Application No. 10/158,773, filed on May 31, 2002, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING, Inventors: van der Goes *et al.*, which is a Continuation-in-Part of Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER *et al.*; and is related to Application No. 10/158,774, Filed: May 31, 2002, Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER *et al*; Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. 10/158,193, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan MULDER *et al.*, all of which are incorporated by reference herein.--

Please insert the following after paragraph [0024]:

--FIG. 10 shows the circuit of FIG. 2 with FET transistors used as switches.

FIG. 11 shows cascaded coarse and fine amplifier stages.--

Please substitute the following paragraph [0028] for the pending paragraph [0028]:

--In one embodiment, 30 coarse amplifiers, 30 coarse comparators, 19 fine amplifiers and 65 fine comparators are used.) The coarse amplifier  $A_C$  is connected to a capacitor  $C_1$ , which in turn is connected to either the output of a track-and-hold 101, or to  $V_{coarse}$  from the reference ladder 104. A two-phase clock, including phases  $\phi_1$  and  $\phi_2$ , is used to control switches  $S_1$ ,  $S_2$  and  $S_3$  of the coarse amplifier  $A_C$ . When the phase  $\phi_1$  is on, the switches  $S_2$  and  $S_3$  are closed, the switch  $S_1$  is open. With the switch  $S_3$  closed, the coarse ADC amplifier

$A_C$  is in a reset mode, and the capacitor  $C_1$  is connected to the reference ladder tap  $V_{coarse}$ . Also on  $\phi_1$ , the switch  $S_5$  is closed, the switches  $S_4$  and  $S_6$  are open, and the fine capacitor  $C_2$  is connected to an appropriate tap of the reference ladder  $V_{fine}$ . Note that all of the switches as  $S_1$ - $S_6$  are typically field effect transistor (FET) switches (see FIG. 10, where the switches are  $S_1$ - $S_6$  illustrated as FET devices). The switch  $S_3$  may be referred to as a coarse ADC reset switch, and the switch  $S_6$  may be referred to as a fine ADC reset switch. When the phase  $\phi_1$  of the two-phase clock is on, the switches  $S_3$  and  $S_2$  are closed, the amplifier  $A_C$  is in a reset mode, and the left side of the capacitor  $C_1$  is connected to a tap of the reference ladder (i.e.,  $V_{coarse}$ ). The switch  $S_1$  is open when  $\phi_1$  is on.--

Please substitute the following paragraph [0043] for the pending paragraph [0043]:

-- FIG. 4 further illustrates the operation of the amplifiers of the present invention in a situation where the fine ADC 105 has 4 cascaded stages (typically with a gain of 4x each), which are labeled GA, GB, GC and GD. (See FIG. 11, where two cascaded stages are shown for both fine and coarse amplifiers  $A_F$  and  $A_C$ , as one example.) In FIG. 4, the amplifier stage of the coarse ADC 102 is labeled GE, the coarse ADC comparator 107 is labeled CC, the fine ADC comparator 108 is labeled FC and the encoder is labeled ENC. The gray portions of FIG. 4 illustrate a progression of one sample's quantization down the amplifier cascade. First, the track-and-hold 101 is connected to the coarse ADC amplifier  $A_C$ , during phase  $\phi_2$ . Meanwhile, the coarse comparator 107 (CC) is reset during  $\phi_2$ . The fine ADC amplifier  $A_F$  stage GA is also reset. During the next phase  $\phi_1$ , the first stage GA of the fine ADC 105 amplifies, while the second stage GB resets. The process continues, as the signal moves in a pipelined manner down from GA to GB to GC to GD to the fine comparator 108 (FC), and ultimately to the encoder 106. The next quantization is directly behind the quantization just performed, moving from left to right in the figure, and offset by one clock cycle from the measurement illustrated in gray in FIG. 4.--

***In the figures:***

A corrected FIG. 4, and new FIGS. 10-11 are submitted.

***In the claims:***

Please cancel claims 21-31 and 33 without prejudice or disclaimer.

Please substitute the following claims 1, 6-8, 11-20 and 32-33 for the pending claims 1, 6-8, 11-20 and 32-33:

1. (Amended) An analog to digital converter (ADC) comprising:
  - a first amplifier tracking an input voltage with its output;
  - a coarse ADC amplifier connected to a coarse capacitor at its input and having a coarse ADC reset switch controlled by a first clock phase;
  - a fine ADC amplifier connected to a fine capacitor at its input and having a fine ADC reset switch controlled by a second clock phase, wherein a set of reference voltages is selected for use by the fine ADC amplifier based on an output of the coarse ADC amplifier,
  - wherein the coarse capacitor is charged to a coarse reference voltage during the first clock phase and connected to the first amplifier's output voltage during the second clock phase, and
  - wherein the fine capacitor is connected to a fine reference voltage during the first clock phase and charged to the first amplifier's output voltage during the second clock phase; and
  - an encoder that converts outputs of the coarse and fine ADC amplifiers to a digital output.

6. (Amended) The analog to digital converter of claim 1, wherein the coarse capacitor is connected to the first amplifier's output on a delayed second phase.

7. (Amended) The analog to digital converter of claim 1, wherein the fine ADC capacitor is connected to the first amplifier's output on a delayed second clock phase and to the fine reference voltage during a delayed first clock phase.

8. (Amended) The analog to digital converter of claim 1, further including a switch that connects an output of the first amplifier to the coarse capacitor on the second clock phase.

11. (Amended) An analog to digital converter comprising:  
a track-and-hold amplifier tracking an input voltage;  
a first plurality of amplifiers each connected to a corresponding capacitor at its input, wherein the amplifiers of the first plurality are reset on a clock phase  $\phi_1$  and their corresponding capacitors are connected to an output of the track-and-hold on a clock phase  $\phi_2$ ;

a second plurality of amplifiers each connected to a corresponding capacitor at its input, wherein the amplifiers of the second plurality are reset on the clock phase  $\phi_2$  and their corresponding capacitors are charged to the track-and-hold amplifier output voltage on the clock phase  $\phi_2$  and wherein a set of reference voltages is selected based on outputs of the first plurality of amplifiers, for input to the second plurality of amplifiers on the clock phase  $\phi_1$ ; and

an encoder that converts outputs of the first and second pluralities of amplifiers to a digital output.

12. (Amended) The analog to digital converter of claim 11, further including FET switches that reset the first plurality of amplifiers on the clock phase  $\phi_1$ .

13. (Amended) The analog to digital converter of claim 11, wherein the clock phases  $\phi_1$  and  $\phi_2$  are non-overlapping.

14. (Amended) The analog to digital converter of claim 11, wherein each of the second plurality of amplifiers includes a plurality of cascaded amplifier stages.

15. (Amended) The analog to digital converter of claim 11, wherein each of the first plurality of amplifiers includes a plurality of cascaded amplifier stages.

16. (Amended) The analog to digital converter of claim 11, wherein the capacitors of the first plurality of amplifiers are connected to the track-and-hold amplifier output on a delayed clock phase  $\phi_2$ .

17. (Amended) The analog to digital converter of claim 11, wherein the capacitors of the second plurality of amplifiers are connected to the track-and-hold amplifier output on a delayed clock phase  $\phi_2$ , and to the set of reference voltages on a delayed clock phase  $\phi_1$ .

18. (Amended) The analog to digital converter of claim 11, further including switches that connect an output of the track-and-hold to the capacitors of the first plurality of amplifiers on the clock phase  $\phi_2$ .

19. (Amended) The analog to digital converter of claim 11, further including a first plurality of comparators that latch the outputs of the first plurality of amplifiers and output them to the encoder.

20. (Amended) The analog to digital converter of claim 19, further including a second plurality of comparators that latch the outputs of the second plurality of amplifiers and output them to the encoder.

32. (Amended) An analog to digital converter comprising:  
a track-and-hold amplifier tracking an input voltage;  
a first amplifier that resets on a clock phase  $\phi_1$  and amplifies a difference of an output of the track-and-hold amplifier and a first voltage reference on a clock phase  $\phi_2$ , wherein the track-and-hold amplifier is in a hold-mode on the clock phase  $\phi_2$ ;

a second amplifier that resets on the clock phase  $\phi_2$  and amplifies a difference of the output of the track-and-hold amplifier and a second reference voltage on the clock phase  $\phi_1$ , wherein a first set of reference voltages is selected for use by the second amplifier based on an output of the first amplifier; and

an encoder that converts outputs of the first and second amplifiers to a digital output.

33. (Amended) A method of converting an analog voltage to a digital voltage comprising the steps of:

resetting a first amplifier on a first clock phase;

charging a first capacitor to a first reference voltage during the first clock phase;

connecting the first capacitor to an input voltage during a second clock phase

wherein a track-and-hold amplifier is in a hold-mode during the second clock phase;

selecting a second reference voltage based on an output of the first amplifier;

connecting a second capacitor to the second reference voltage during the first clock phase;

charging the second capacitor to the input voltage during the second clock phase;

amplifying a voltage on the first capacitor on the second clock phase;

resetting a second amplifier on the second clock phase;

amplifying a voltage of the second capacitor on the first clock phase; and

converting outputs of the first and second amplifiers to a digital output.

Please add new claims 35-40 as follows:

35. (New) The analog to digital converter of claim 1, wherein the first amplifier is in a hold-mode during the second clock phase.

36. (New) The analog to digital converter of claim 1, further including a switch matrix to select the set of reference voltages for use by the fine ADC amplifier.

37. (New) The analog to digital converter of claim 11, wherein the track-and-hold amplifier is in a hold-mode on the clock phase  $\phi_2$ .

38. (New) The analog to digital converter of claim 11, further including a switch matrix to select the set of reference voltages based on the outputs of the first plurality of amplifiers.

39. (New) The analog to digital converter of claim 32, wherein the track-and-hold amplifier is in a hold-mode during the clock phase  $\phi_2$ .

40. (New) The analog to digital converter of claim 32, further including a switch matrix to select the set of reference voltages for use by the second amplifier.